Amendments to the Specification

Please replace the Abstract with the following:

ABSTRACT OF THE DISCLOSURE

A built-in self test (BIST) circuit ~~comprising~~ is provided, where the circuit includes ~~a linear feedback shift register is disclosed. The BIST circuit comprises~~ a controller for controlling a self-testing operation of a memory chip embedded in an integrated circuit, an address generator for generating pseudo-random address patterns under control of the controller, a data generator for producing test data associated with data backgrounds of the address bits under the control of the controller, and a comparator for comparing the test data with memory data output from the memory chip to detect a defect, if any, of the memory chip. ~~The pseudo-random random pattern comprises a single random pseudo-random address pattern.~~

Please change the paragraph beginning on page 7, line 20 and ending on page 8, line 3, with the following:

The test data DI is written to a memory cell of memory 150 corresponding to the test address. The comparator 140 compares the test data DI with memory data DO read from the memory 150 to produce a detection signal P/F (Pass/Fail). The detection signal P/F is applied to the BIST controller 110. The detection signal is active depending on a predetermined condition. For example, the detection signal may be active upon coincidence of the two data ~~DL~~ DI and DO and inactive when the two data ~~DL~~ DI and DO are not coincident.